REMARKS

Reconsideration of the application is requested.

Claims 1-20 remain in the application. Claims 1-20 are subject to examination. Claims 1 and 11 have been amended.

In item 3 on pages 2-6 of the above-identified Office Action, claims 1-6, 8, 11-15, 18 and 20 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) under 35 U.S.C. § 103.

In the Office Action, the Examiner explicitly equates (see page 3 of the Office Action):

- the table memory recited in amended claim 1 of the instant application with the base address register 18 of Tipon;

- the digital processor recited in amended claim 1 with the processor 12 of Tipon; and

- the computation rule in hardware recited in amended claim 1 with the ALU 24 of Tipon.

Amended claim 1 of the instant application additionally recites the steps of:

> preselecting a base address in the table memory dependent on a data type of data to be transmitted;
>
> computing a plurality of addresses according to a prescribed arithmetic computation rule in hardware by taking the preselected base address as a starting point resulting in computed plurality of addresses; and
>
> accessing the table memory with the digital processor using the computed plurality of addresses for consecutive read access operations and/or consecutive write access operations in the table memory (emphasis added).

Accordingly, these method steps are only disclosed by Tipon, **if** the processor 12 accesses the base address register 18 by **using the addresses computed by the ALU 24** (and stored in the real address output register 44). In this context the Examiner cites the text passage column 3, lines 15 to 32, that discloses the base address register 18 to be loaded by the processor 12 with a base address over the bus 14 under the control of the processor 12 via the address bus 16. Further, the loading of the base address is performed according to a computer program. The cited text passage of Tipon does not disclose the above

recited method steps of the instant application for the now described reasons.

First, the base address register 18 of Tipon is loaded with a **base address**. The ALU 24, however, calculates **physical addresses** that are stored in the **register 44**. These physical addresses are calculated by combining base addresses and offset addresses (see column 4, lines 1 to 15) and therefore **do not** correspond to base addresses. Consequently, the base address register 18 is **not** accessed by using the addresses computed by the ALU 24 as recited in amended claim 1 of the instant application and therefore Tipon cannot read on amended claim 1.

Second, the loading of the base address register 18 in Tipon is performed according to a **computer program** stored in the main memory (not shown). Tipon does not disclose any coupling or functional relationship between the computer program and the register 44. Thus, **no usage** of the physical addresses stored in the register 44 to access the base address register 18 occurs in Tipon but are clearly recited in amended claim 1 of the instant application.

Third, Tipon discloses the physical addresses stored in

the register 44 to be forwarded to an external main memory (see right hand side of Fig. 1, ***"TO MAIN MEMORY ADDRESS BUS"***). Thus, no usage of the physical addresses **by the processor 12** as required by amended claim 1 is disclosed in Tipon.

It is an object of the invention of the instant application to provide a method for transmitting data between a digital processor and a hardware arithmetic-logic unit. In contrast to this, Tipon relates to the field of offset addressing. A data transmission according to the invention of the instant application cannot be established by means or a device as disclosed by Tipon. Therefore, the technical scheme of Tipon does not prompt a person of average skill in the art to arrive at the subject matter of amended claim 1 of the instant application.

Newly amended independent claim 11 of the instant application features a similar technical scheme as the amended claim 1. Accordingly, the novelty and inventiveness of claim 11 can be justified by the same arguments recited above with regard to claim 1 and are therefore not repeated here.

In item 4 on pages 6-7 of the above-identified Office Action, claim 7 has been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 3,833,888 to Stafford et al. (hereinafter Stafford) under 35 U.S.C. § 103.

The Examiner alleges that the subject matter of the claim 7 of the instant application is disclosed by Stafford and in this regard refers to the Abstract of Stafford. Stafford is not believed to disclose (neither in the abstract nor in the rest of the document) the usage of channel decoding or any specifications on logic implementations of the digital processor, thereby determining how many soft input values per unit time can be stored. Thus the subject matter of claim 7 cannot be disclosed by Stafford.

In item 5 on pages 7-8 of the above-identified Office Action, claims 9-10 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No.

6,310,891 to Dove et al. (hereinafter Dove) under 35 U.S.C. § 103.

Claim 9 of the instant application recites "*choosing a packing mode causing a plurality of data words, output by the processor for performing the step of accessing the table memory, to be combined to form a memory data word for the table memory*". The Examiner finds the subject matter of claim 9 to be disclosed by Dove. Dove concerns a method of scheduling a plurality of time multiplexed cells and a plurality of asynchronous cells in a temporal frame. The concrete structure of the temporal frame is illustrated in Fig. 1. However, Dove does not disclose a processor outputting data words to be packed and a table memory for which the combined data word is provided. A similar argumentation is valid for claim 10, which requires the choice of an unpacking mode.

In item 8 on pages 9-10 of the above-identified Office Action, claims 16-17 have been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 6,363,119 to Oami (hereinafter Oami) under 35 U.S.C. § 103.

Claim 16 of the instant application recites "*a multiplexer and buffer device for assembling* a *plurality of data words output by said processor to form* a *memory data word intended for being stored at an address in said table memory*". The Examiner asserts that the subject matter of claim 16 is disclosed by Oami, thereby citing column 25, lines 51 to 61, in connection with Fig. 5. Fig. 5 shows a multiplexer 95 receiving data from an arithmetic coding section 91 (identified as processor), which is, stored in a buffer of the multiplexer 95. However, Oami does not disclose the formed data (identified as enhancement layer bit-stream, see right hand side of Fig. 5) to be intended for being stored in a table memory. A similar argumentation is valid for claim 17 of the instant application, which contrarily requires the usage of a multiplexer (see Fig. 4 concerning this matter).

In item 7 on pages 10 and 11 of the above-identified Office Action, claim 19 has been rejected as being obvious over U.S. Patent No. 4,405,980 to Hess (hereinafter Hess) in view of U.S. Patent No. 5,150,471 to Tipon et al. (hereinafter Tipon) and further in view of U.S. Patent No. 5,311,523 to Serizawa et al. (hereinafter Serizawa) under 35 U.S.C. § 103.

Claim 19 ultimately depends from claim 11, and since claim 11 is believed to be allowable for the above-stated reasons, claim 19 is also believed to be allowable.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1 or 11. Claims 1 and 11 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claim 1 or 11.

In view of the foregoing, reconsideration and allowance of claims 1-20 are solicited.

Please charge any other fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

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